REMARKS

By the present amendment and response, new claims 93-117 have been added to overcome the art cited by the Examiner and claims 65-92 have been canceled. Thus, claims 93-117 are pending in the present application. Reconsideration and allowance of pending claims 93-117 in view of the following remarks are requested.

For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by new independent claims 93 and 105, is patentably distinguishable over U.S. patent number 5,792,706 to Michael et al. ("Michael") in combination with U.S. patent number 5,798,559 to Bothra et al. ("Bothra") and U.S. patent number 6,040,248 to Chen et al. ("Chen").

The present invention, as defined by new independent claim 93, defines a method of manufacturing an interconnect comprising steps of forming a first patterned layer of conductive material having at least one trench, depositing a first insulating layer over the first patterned layer and filling the at least one trench, depositing a first hard mask on the first insulating layer, forming first and second air gaps and a support pillar in the first hard mask and first insulating layer, where the support pillar is situated between the first and second air gaps, and depositing a sealing layer over the first hard mask. As disclosed in the present application, by forming first and second air gaps at appropriate locations in the first hard mask and first insulating layer, the present invention provides an interconnect structure that advantageously achieves reduced parasitic capacitance between interconnect lines, i.e. intra-layer capacitance, and/or between interconnect

layers, i.e. inter-layer capacitance. For example, by situating first and second air gaps in the at least one trench, parasitic capacitance between interconnect lines can be reduced. By way of another example, by situating first and second air gaps over an interconnect line in the first patterned layer of conductive material, the present invention can be advantageously employed to reduce inter-layer parasitic capacitance.

Furthermore, as disclosed in the present application, the support pillar can be appropriately situated adjacent to an interconnect line in the first patterned layer of conductive material to increase the mechanical strength and thermal conductivity of the interconnect line. In addition, as disclosed in the present application, the hard mask is utilized during etch and clean steps in transferring an air gap pattern to the first insulating layer to precisely determine the location of the first and second air gaps. Thus, the present invention advantageously achieves a flexible interconnect structure that includes first and second air gaps to provide reduced inter-layer and/or intra-layer parasitic capacitance and a support pillar situated between the first and second air gaps to increase mechanical strength and thermal conductivity of an adjacent interconnect line.

Moreover, new independent claim 105 of the present application defines a method comprising steps of forming a first patterned layer of conductive material having at least one trench, depositing a first insulating layer over the first patterned layer and filling the at least one trench, depositing a second insulating layer over the first insulating layer, depositing a first hard mask on the first insulating layer, forming first and second air gaps and a support pillar in the first hard mask, second insulating layer, and first insulating

layer, where the support pillar is situated between the first and second air gaps, and depositing a sealing layer over the first hard mask.

As disclosed in the present application, by utilizing first and second insulating layers, the present invention achieves a flexible interconnect structure that can be advantageously adapted to satisfy the requirements of specific applications. For example, the first insulating layer may be a gap fill silicon dioxide layer that can be deposited by a high-density plasma chemical vapor deposition process, while the second insulating layer may be a bulk silicon dioxide layer that may be deposited by a plasma-enhanced chemical vapor deposition process. By way of further example, the first insulating layer may comprise a material having a low dielectric constant and the second insulating layer may comprise an oxide. The present invention, as defined by new independent claim 105, also includes the advantages of new independent claim 93 discussed above.

In contrast, Michael does not teach, disclose, or suggest a method of manufacturing an interconnect structure comprising steps of depositing a first hard mask on a first insulating layer and forming first and second air gaps and a support pillar in the first hard mask and first insulating layer, where the support pillar is situated between the first and second air gaps. Michael specifically discloses a method for forming an interlevel dielectric including removing portions of first dielectric 20 to form air gap trenches 26 in first dielectric 20. See, for example, column 6, lines 12-14 and Figures 5-7 of Michael. Capping dielectric 30 is formed over first dielectric 20, which results in cusping that serves to seal off the upper portion of trenches 26 without filling trenches 26

with dielectric material. See, for example, Michael, column 6, lines 57-66. Thus, the interlevel dielectric disclosed in Michael includes air gap trenches 26 formed in first dielectric 20, where the upper portion of air gap trenches 26 are sealed off by capping dielectric 30.

In contrast to the present invention as defined by new independent claims 93 and 105, Bothra does not teach, disclose, or suggest a method of manufacturing an interconnect structure comprising steps of depositing a first hard mask on a first insulating layer and forming first and second air gaps and a support pillar in the first hard mask and first insulating layer, where the support pillar is situated between the first and second air gaps. Bothra specifically discloses forming an interconnect structure having air as a dielectric by removing sacrificial oxide layers by isotropic etchant 162 to form regions 180, which have air as a dielectric. See, for example, column 8, lines 32-38 and Figure 4 of Bothra.

In contrast to the present invention as defined by new independent claims 93 and 105, Chen does not teach, disclose, or suggest a method of manufacturing an interconnect structure comprising steps of depositing a first hard mask on a first insulating layer and forming first and second air gaps and a support pillar in the first hard mask and first insulating layer, where the support pillar is situated between the first and second air gaps. Chen specifically discloses a method for etching contact/via openings in organic dielectric layers by patterning silicon oxide layer 52 by photoresist layer 54 to define via opening 60. See, for example, column 6, lines 1-17 and Figure 3a of Chen. In Chen,

photoresist layer 54 is used to form a silicon oxide hardmask, which is then utilized to etch a via in organic layer 50. See, for example, Chen, column 6, lines 18-21. For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by new independent claims 93 and 105, is not suggested, disclosed, or taught by Michael in combination with Bothra and Chen. As discussed above, new independent claims 93 and 105 are patentably distinguishable over Michael in combination with Bothra and Chen and, as such, claims 94-104 depending from new independent claim 93 and claims 106-117 depending from new independent claim 105 are, a fortiori, also patentably distinguishable over Michael in combination with Bothra, and Chen.

Based on the foregoing reasons, the present invention, as defined by new independent claims 93 and 105 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 93-117 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 93-117 pending in the present application is respectfully requested.

Respectfully Submitted,
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